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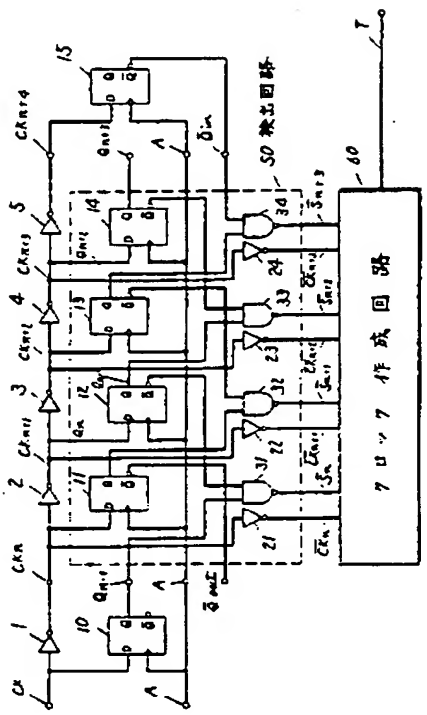
TITLE : CLOCK GENERATOR



ABSTRACT : PURPOSE: To make the operation stable by using a clock generating circuit generating a clock subject to phase control from the output of an inverter selected from the result of detection by a detection circuit to apply phase control to the clock.

CONSTITUTION: A clock CK before phase control is applied is inputted and inverted and retarded by inverters 1~5. The clock CK and inverted and inverted and retarded clocks CK_n~CK_{n+4} are latched simultaneously at flip-flops 11~14 in a detecting circuit 50, a 1st stage flip-flop 10 and the final stage flip-flop 15 by using a synchronizing pulse A, respectively. Then a proper clock is detected from outputs of a flip-flop of a stage and that after two-succeeding stages only at the leading edge with respect to the D input. A clock generating circuit 60 generates a clock T whose leading time is coincident with the pulse A by using a clock output, inverse of CKm and a detection output, inverse of Sm. Thus, stable clock phase control is attained.